



FIG 1 (Prior Art)

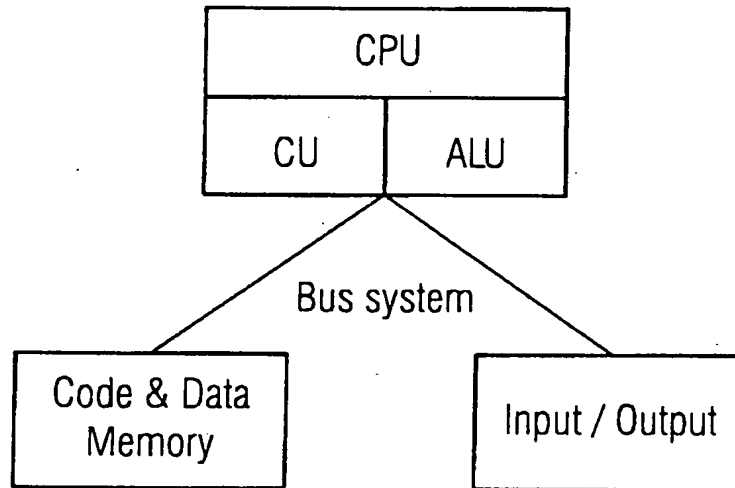


FIG 2 (Prior Art)

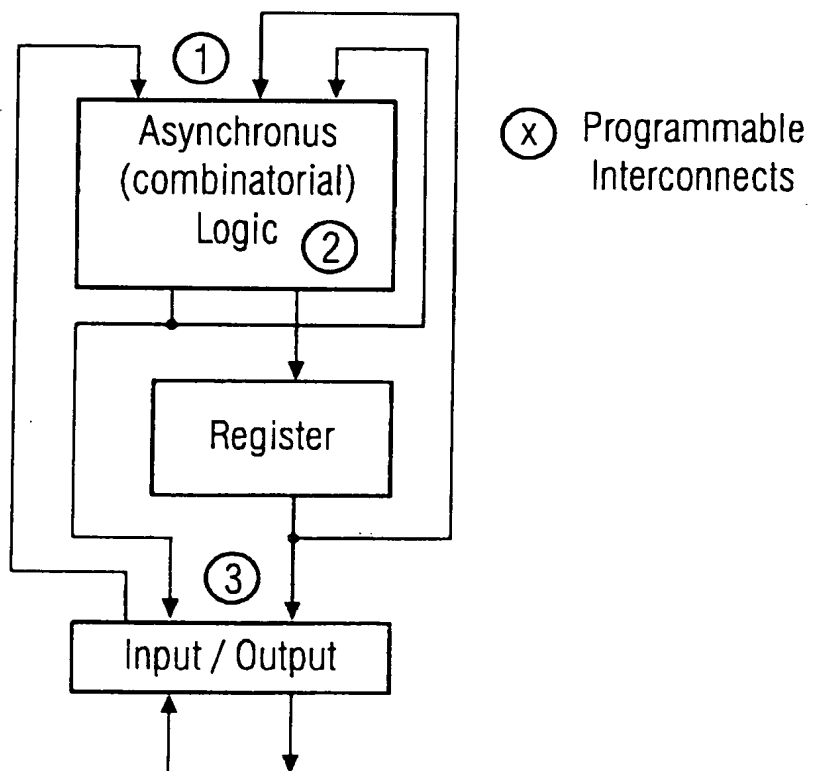




FIG 3 (Prior Art)

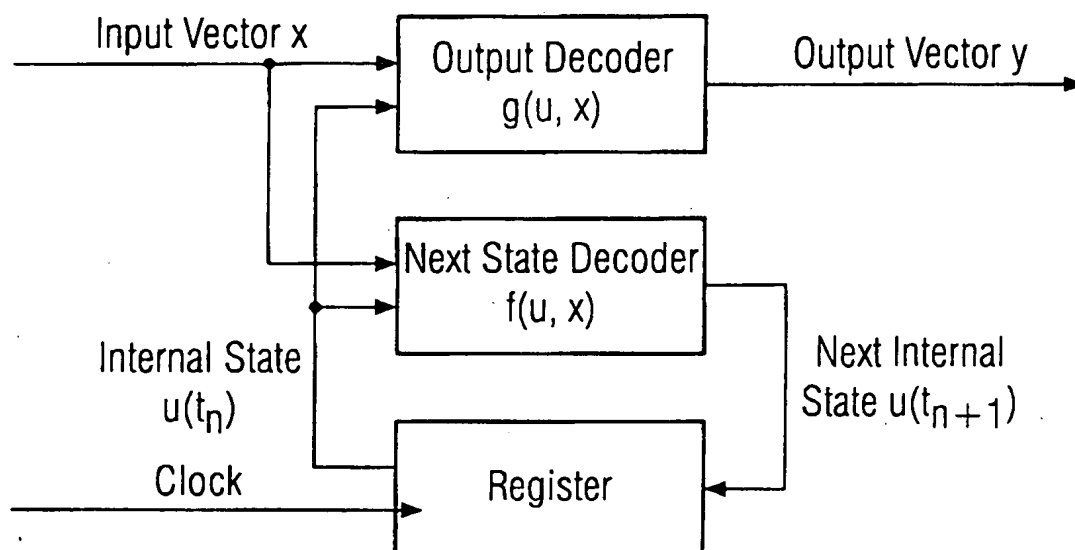


FIG 4

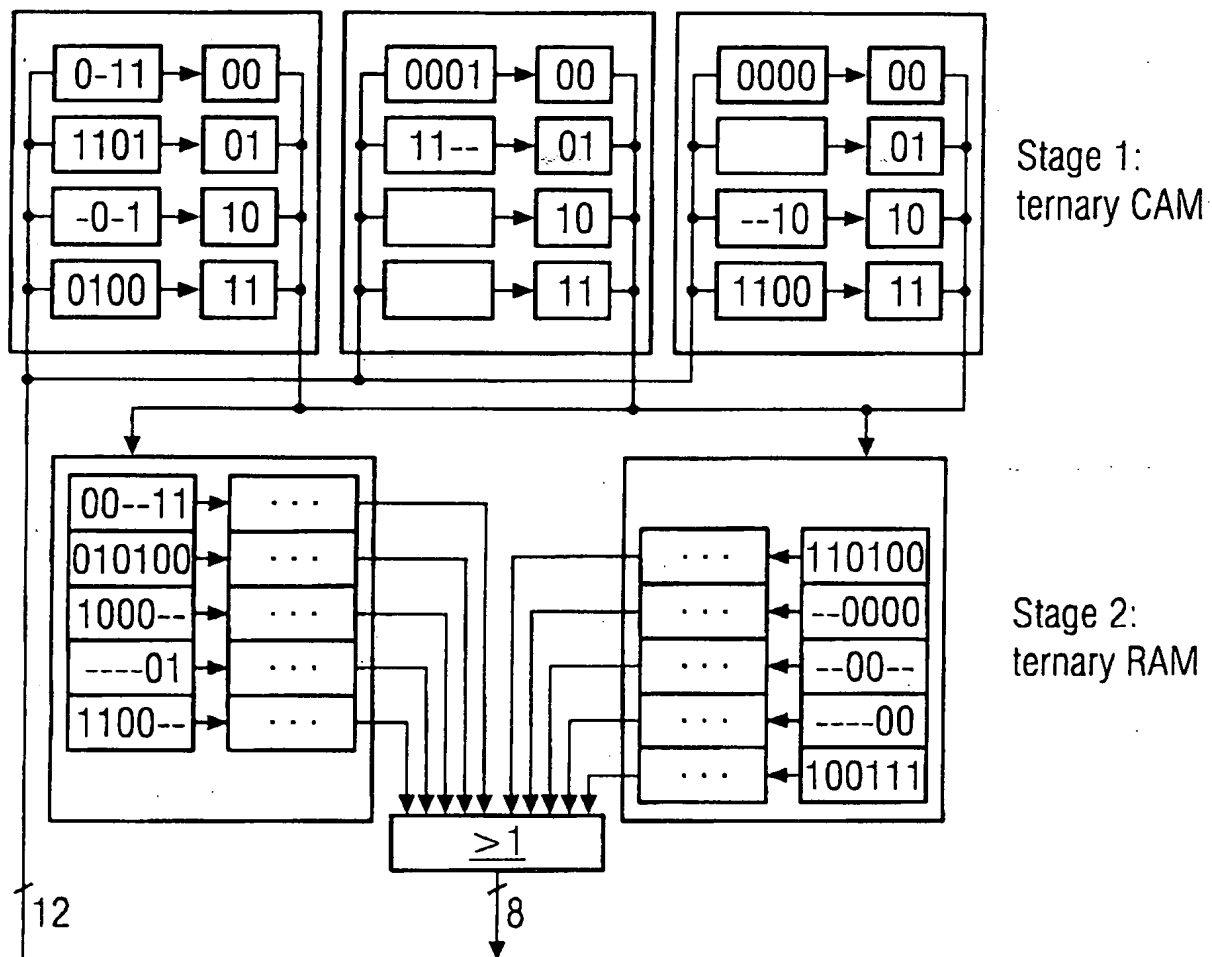




FIG 5a

partial
Minterms
Bits 0-3

1. 0-11
2. 1101
3. -0-1
4. ----
5. 0100
6. 0100
7. ----
8. ----
9. ----
10. -0-1

FIG 5b

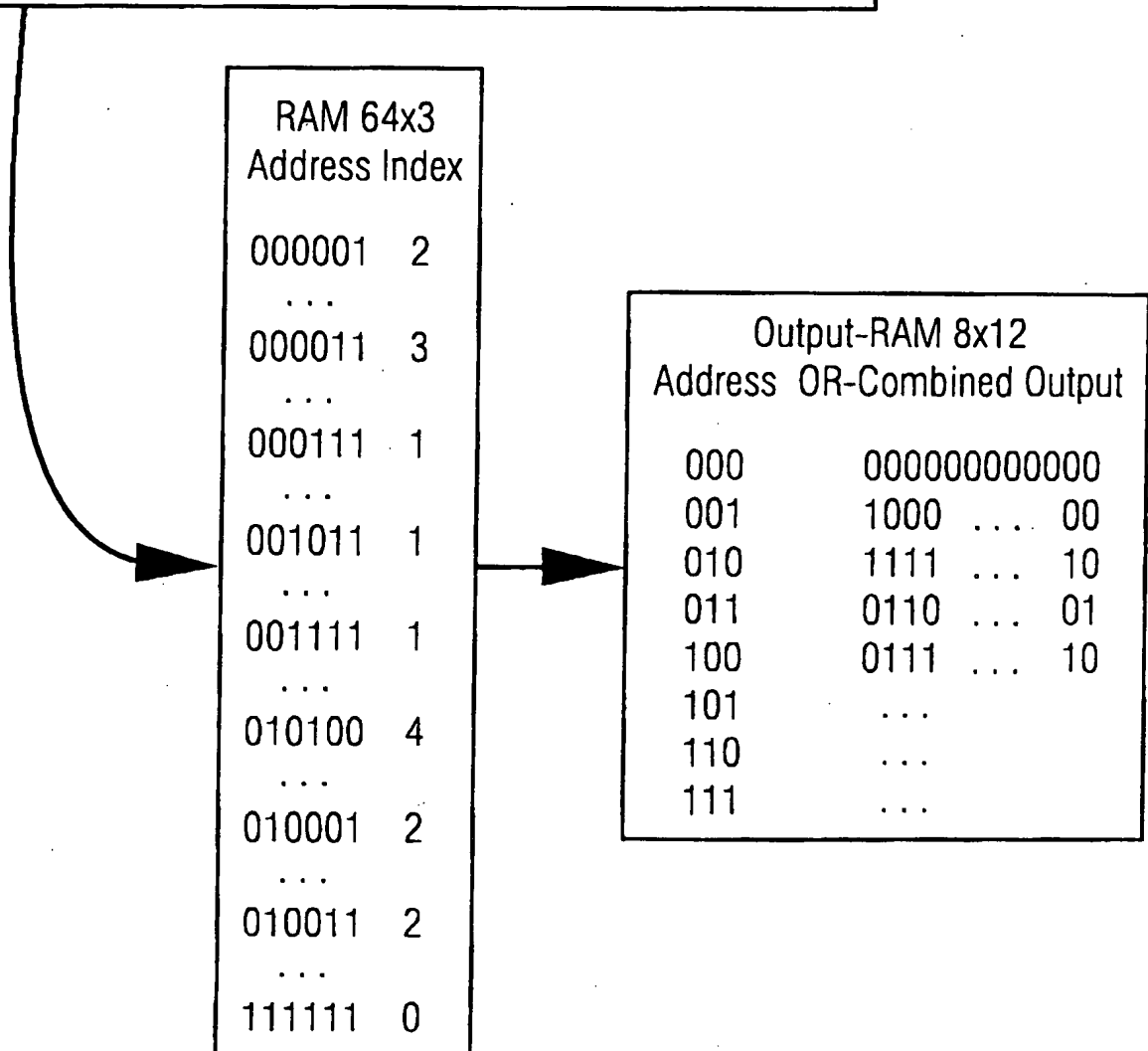
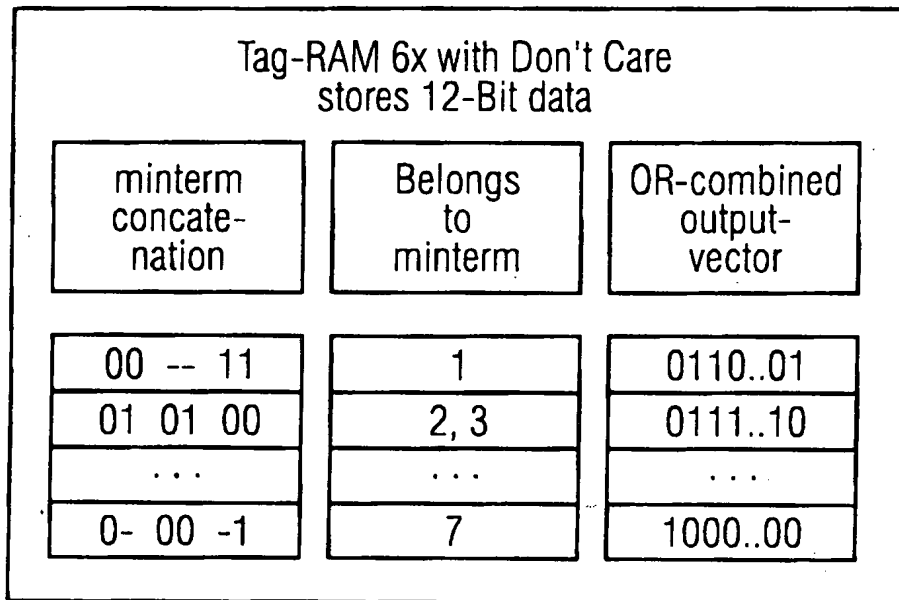
Tag-RAM incl. Don't Care	
Tag	Code
0-11	0
1101	1
-0-1	2
0100	3

FIG 5c

RAM 16x4 Address Code	
0000	8
0001	2
0010	8
0011	4
0100	3
0101	8
0110	8
0111	0
1000	8
1001	2
1010	8
1011	2
1100	8
1101	1
1110	8



FIG 6





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FIG 7

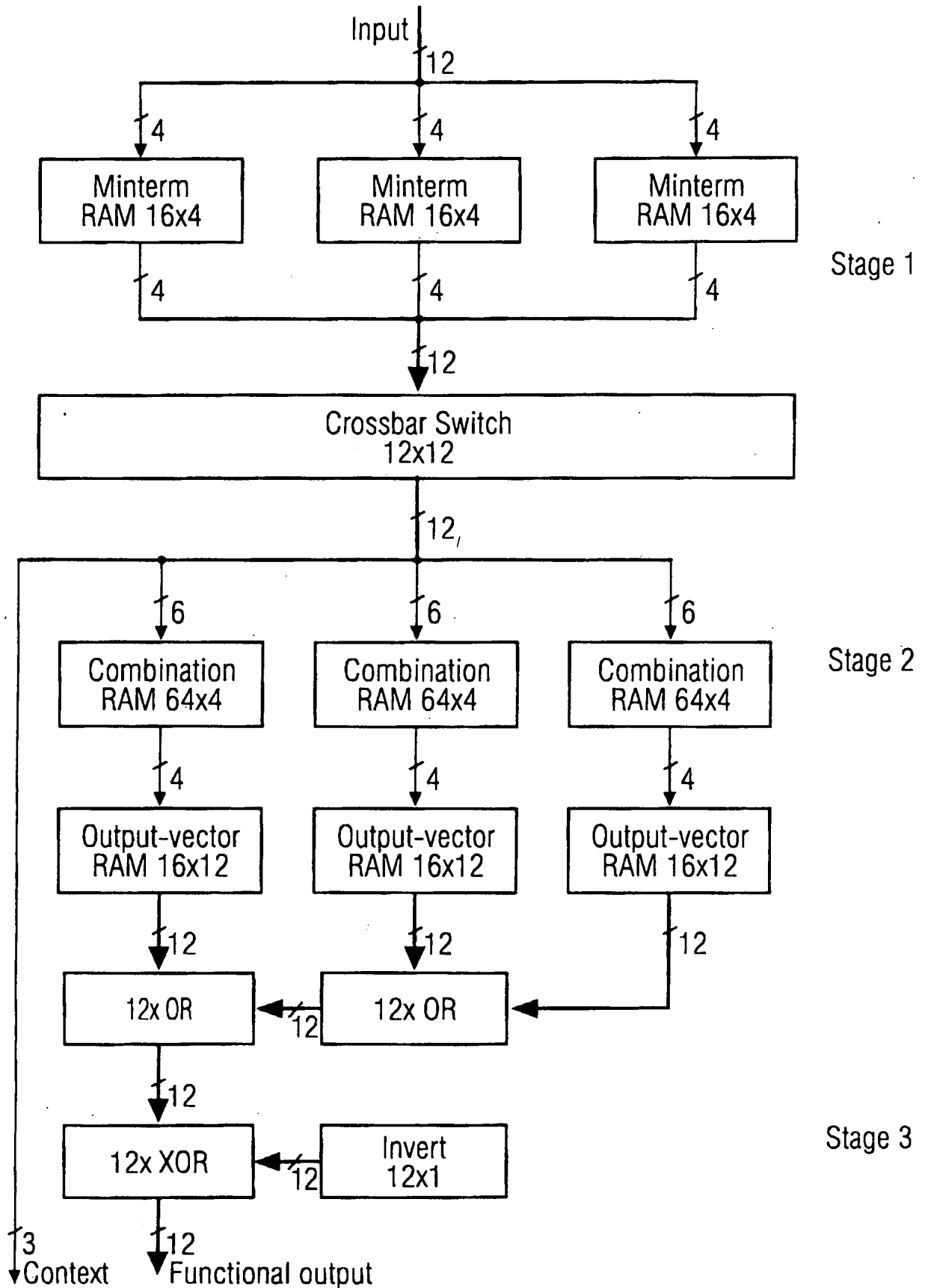




FIG 8

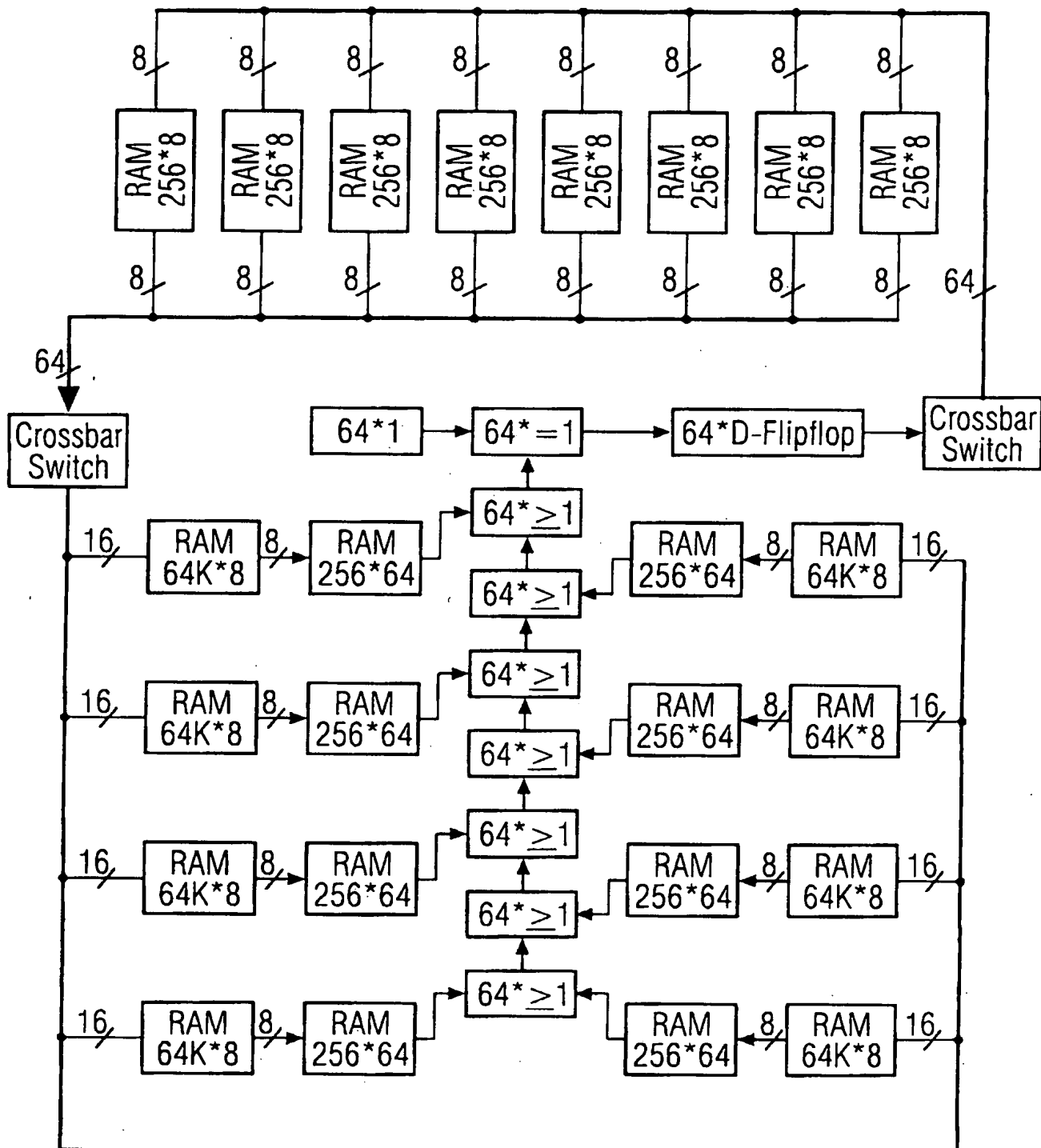




FIG 9

